(19) Europäisches Patentamt
European Patent Office
Office européen des brevets

(11) EP 1 148 548 A2

(12) EUROPEAN PATENT APPLICATION

(43) Date of publication:
24.10.2001 Bulletin 2001/43

(51) Int Cl.[7]: **H01L 23/485**

(21) Application number: **01302292.6**

(22) Date of filing: **13.03.2001**

(84) Designated Contracting States:
AT BE CH CY DE DK ES FI FR GB GR IE IT LI LU MC NL PT SE TR
Designated Extension States:
AL LT LV MK RO SI

(30) Priority: **19.04.2000 US 552560**

(71) Applicant: **Advanced Interconnect Technology Ltd.**
Tsuen Wan, Hong Kong (HK)

(72) Inventors:
- **Cheung, Edwin Wai Ming**
  Tsuen Wan, Hong Kong (HK)
- **Karim, Zaheed Sadrudin**
  New Territories Hong Kong (HK)

(74) Representative:
Watkin, Timothy Lawrence Harvey
Lloyd Wise, Tregear & Co.,
Commonwealth House,
1-19 New Oxford Street
London, WC1A 1LW (GB)

(54) Method of forming lead-free bump interconnections

(57) A method of forming solder bumps on a chip or wafer for flip-chip applications comprises the steps of providing a chip or wafer having a plurality of metal bonds pads which provide electrical connection to the chip or wafer, and applying a solder bump comprising pure tin or a tin alloy selected from tin-copper, tin-silver, tin-bismuth or tin-silver-copper by an electroplating technique, and melting the solder bumps by heating to a temperature above the bump melting point to effect reflow.

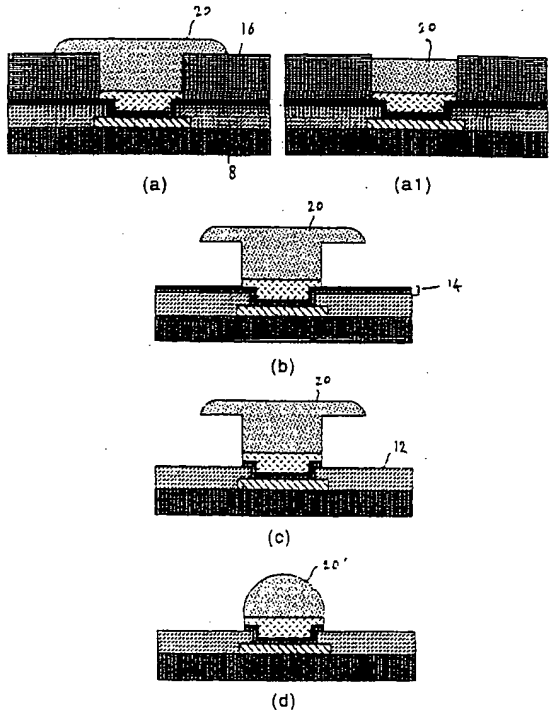


FIG. 3

EP 1 148 548 A2

Description

Background of the Invention

[0001] The present invention relates to a method of forming lead-free solder bump interconnections on semiconductor wafers for flip-chip bonding applications.

[0002] With flip-chip interconnect technology, a raised electrically conductive contact called a "bump" is first formed onto the input/output connection pads of an integrated circuit (IC) which is subsequently assembled face-down (or "flip-chip" bonded) without the use of conventional wire bonds or leads. Various bump interconnection media have been proposed including gold, lead-tin solder, nickel, copper, and conductive polymers. Lead-tin bumps are particularly attractive due to the self-alignment and self-planarizing properties (upon reflow) of solder which allows for a more robust and manufacturable attachment process. In addition to providing electrical contact, the solder bump also forms a mechanical, and thermal connection between the chip and substrate. The use of lead-tin solder bumps for flip-chip applications was first introduced by IBM in the 1960's in their C4 (controlled-collapse-chip-connection) technology using a method of evaporation for fabrication of the bumps.

[0003] Primary advantages of flip-chip technology as compared to other interconnection techniques include:

i) the capacity to significantly increase the total number of connections that can be made to the chip because the small bump contacts can be placed virtually anywhere on the surface of the chip and at points convenient for a particular application (unlike "perimeter-only" bonding technologies such as wire-bonding and tape-automated-bonding (TAB));
ii) the potential to shrink the die size and obviate the need for long metallization lines leading to the periphery pads which would favourably impact both the IC manufacturing yield and reliability;
iii) lower electrical resistance and inductance values leading to faster interconnection speeds and lower power consumption;
iv) better thermal dissipation performance due to conduction through the solder bumps and exposed rear surface of the IC after flip-chip bonding;
v) provision for a smaller, lighter, and more compact package with overall lower packaging cost per pin.

[0004] The selection of the precise composition of a solder bump material is conventionally influenced by a variety of factors, most particularly melting point. Attention must be paid to the solder melting point, particularly where the chip is bonded to a substrate which are mostly formed of low-cost organic materials with relatively low Tg (glass transition temperatures). When the IC is flip-chip bonded, it is normally heated to a temperature which is typically 20-30°C higher than the melting point of the solder. Too high a melting point for the solder bump may therefore lead to damage of the substrate.

[0005] The two most common bump materials currently in use for flip-chip bonding applications consist of pure gold and lead-tin based alloys. The former are used mainly to flip-chip a silicon IC onto liquid crystal displays (LCDs) or in TAB packages. Lead-tin solder bumps are used primarily for flip-chip-on-board or flip-chip-in-package applications.

Solder bumps are typically preferred over gold bumps due to their lower cost and self-planarizing and self-aligning reflow characteristics which provides for a more manufacturable and robust flip-chip bonding process.

[0006] Lead-tin alloys commonly employed as solder bumps include in particular 95wt%Pb/5wt%Sn, 97wt%Pb/3wt%Sn, and eutectic 37wt%Pb/63wt%Sn. Lead-based solders with additions of In, Ag, and Bi have also been proposed.

[0007] With growing environmental awareness, a worldwide ban on the use of lead-containing solders in electronic products is under consideration since the lead from such products, which are typically disposed of in landfills, eventually leaches into the drinking water system. Laws restricting the use of lead in electronics products may be enacted in the European Community, and similar legislation to ban lead is pending in the United States and in Japan. Efforts to identify suitable lead-free finishes for electronic components has thus far been focused mainly on printed circuit boards, leadframe packages, and in the selection of solder pastes. Little attention has been paid to the fabrication of bump interconnections for flip-chip applications.

[0008] Lead-free solders have been proposed including those based on indium and its alloys with bismuth, tin, antimony, zinc and silver.

[0009] What is required are lead-free solder bump compositions which can be directly substituted for the lead-tin alloys conventionally used for flip-chip applications, and a fabrication method employing such a lead-free solder bump composition.

[0010] It is proposed in US Patent No. 5410184 assigned to Motorola to utilise a lead-free solder alloy having tin as a predominant component, between 2-8%wt or more preferably 3-5%wt copper and up to 1.5%wt silver. This solder requires the presence of an amount of copper at preferably 3-5%wt so as to retain formation of a certain degree of intermetallics for bond integrity. It is found however that this composition may suffer problems of bond embrittlement owing to an excessive formation of the tin-copper intermetallics.

[0011] The present invention seeks to provide a process for forming solder bumps which overcomes the problems mentioned above.

Summary of the Invention

[0012] According to a first aspect the invention resides in a method of forming solder bumps on a chip or

wafer for flip-chip applications, comprising the steps of providing a chip or wafer having a plurality of metal bonds pads which provide electrical connection to the chip or wafer, and applying a solder bump comprising pure tin or a tin alloy selected from tin-copper, tin-silver, tin-bismuth or tin-silver-copper by an electroplating technique, and melting the solder bumps by heating to a temperature above the bump melting point to effect reflow.

[0013] The solder is more preferably one of pure tin, tin-copper alloy of less than 2% weight copper or more preferably about 0.7% by weight copper, tin-silver alloy having less than 20% by weight silver or more preferably about 3.5% by weight silver, or 10% by weight silver, tin-bismuth having between 5% and 25% by weight bismuth or more preferably about 20% by weight bismuth, or tin-silver-copper alloy having less than 5wt% silver, and preferably about 3.5wt%Ag, less than 2wt% copper and preferably about 0.7wt%Cu, with the balance being tin.

[0014] It is found that pure tin or the tin alloys can be directly substituted for the conventional lead-tin alloys, whilst the solder bumps can be formed using electroplating to give particularly well-defined, regular bumps. The tin-based solders identified are also compatible with existing reflow processes and materials, and with surface mount techniques and equipment.

[0015] In the case of the binary alloys tin-copper, tin-silver and tin-bismuth the elements can be simultaneously co-deposited as the alloy from a single plating solution.

[0016] In an alternative technique the elements can be sequentially deposited from separate plating solutions, which form the requisite alloys on heating during the reflow process. This sequential plating is particularly applicable also to the ternary alloy tin-silver-copper. In this case the alloy is deposited by depositing one or other of tin-copper alloy from a single plating solution by co-deposition, or elemental silver, followed by deposition of the other, the ternary alloy forming on heating. It is also possible to sequentially deposit each of the three elements.

[0017] The chip or wafer may be, before electroplating, provided with a sputtered layer or layers of metal which function as a diffusion barrier, barrier to oxidation, adhesion, and plating contact layer (electrical buss). A layer of thick photosensitive polymer material such as photoresist (negative or positive tone) or dry film with a thickness of between 25 - 200 μm is used to define the location and volume of the solder bumps to be plated. The provision of thick photoresist or dry-film is important to ensure sufficient height and volume of the plated solder bump without causing shorting to the next adjacent bump, and to maintain the necessary stand-off height between the chip and the substrate in order to compensate for differences in thermal coefficients of expansion of the chip and the substrate as well to provide a sufficient gap for underfill material to flow between the chip and the substrate after flip-chip bonding.

[0018] The electroplating of the solder bumps can be carried out using either direct current (DC) or pulsed alternating current. The current and voltage values depend on the size of the wafer and the total exposed surface area to be plated. Preferable DC plating parameters range between 3-5 V with a current of between 0.05-0.1 A. In a preferable pulsed plating cycle voltage alternates between +5 V for about 1 millisecond, a zero voltage portion for about 1 millisecond or less, between -5 to -10 V for 1 millisecond, followed by zero voltage for about 1 millisecond.

[0019] Either rack or fountain plating equipment may be used for plating of the solder on the wafers.

[0020] According to a further aspect the invention resides in a method for forming solder bumps on a chip or wafer for flip-chip applications comprising the steps of: (a) providing a chip or wafer having a passivation layer and a plurality of exposed metallic bond pads; (b) applying at least one solder-wettable metal layer to the bond pad; (c) applying a photosensitive layer to the chip or wafer having openings at the portions of the bond pads; (d) applying a solder comprising pure tin, or a tin alloy selected from tin-copper, tin-silver, tin-bismuth, or tin-silver-copper by an electroplating technique; (e) removing the photoresist layer; and (f) melting the solder bumps to effect reflow.

[0021] The invention also resides in a chip or wafer when formed according to the methods described above.

Brief Description of the Drawings

[0022] Embodiments of the invention are now described, by way of example only, with reference to the following drawings in which:

Figure 1 is a sectional view of a flip-chip in a package;

Figures 2(a) to (d) illustrate the first four stages of deposition of solder bumps;

Figures 3(a) to (d) illustrate the deposition steps subsequent to those of Figures 2(a) to (d);

Figures 4(a) and (b) show scanning electron micrographs of tin-copper bumps formed according to the invention; Figures 5 (a) and (b) show scanning electron micrographs of tin-bismuth bumps formed according to the invention; Figures 6(a) and (b) show scanning electron micrographs of pure tin bumps;

Figure 7(a) and (b) shows scanning electron micrographs of tin-silver bumps according to the invention; and

Figures 8(a) and (b) show scanning electron micrographs of tin-silver-copper bumps according to the invention.

Description of the Preferred Embodiments

[0023] Turning to the drawings, Figure 1 shows an in-

tegrated circuit 2 which is "flip-chip" bonded to a substrate 4 by means of metallized contacts 6 of solder referred to in the art as "bumps". The substrate 4 can be a printed circuit board or an intermediate package such as a Ball Grid Array (BGA) or Chip-Scale-Package (CSP) itself bonded to a printed circuit board 9 through additional solder balls 7 or leads. The package can be formed of organic, ceramic, or metal materials.

[0024] The present invention utilizes metal solders which are substantially lead-free (aside from lead present at an impurity level, typically 10p.p.m being tolerated). It is found that particularly advantageous compositions include pure tin, or tin which includes a small amount of an alloying element such as copper, silver, or bismuth, or both silver and copper. It is found that the incorporation of such an alloying element is effective in lowering the melting point of pure tin, in preventing the formation of whiskers on as-plated deposits, in lowering the surface tension of tin (550 dyne/cm at 232°C), to improve the mechanical properties of tin (such as ductility), and in preventing a phase change of pure tin from 8 to form which occurs below 13°C. This phase change is accompanied by a volume change which leads to a decrease in mechanical strength, as well as compromising bond integrity and strength. The solder bump materials are discussed in further detail below.

[0025] Figures 2(a) to (d) and 3(a)/(al) to (d) illustrate a fabrication process for forming metal solder bump interconnections of the described compositions utilizing an electroplating technique.

[0026] Figure 2(a) shows the semiconductor wafer 8 to which has previously been applied at appropriate locations bond pads, which are conventionally made of Al:Si (1-2wt%Si) or Al:Si:Cu (1-2wt%Si and 1-5wt%Cu), or more recently pure copper, and a glass passivation layer 12 which extends over the wafer, but is removed at appropriate positions to expose the bond pads 10. The bond pads make electrical connection to the active areas of the chips.

[0027] The first step involves cleaning of the wafer 8 by a backsputter process performed under vacuum in order to remove the naturally formed oxide layer on the bond pads. The cleaning step is followed by the sputter deposition of a single or series of metal layers 14 and usually two as indicated in Fig. 2(b). The first metal layer which is typically made of chrome, with a thickness of between 500 - 1000 Å performs a number of functions including increasing adhesion to the cleaned bond pads, and to the glass passivation, preventing re-oxidation of the metal pad and forming a barrier diffusion layer to the solder. Ti/W, NiV or Ti may also be used for the first layer. The second metal layer is formed of copper of thickness 2500-10000Å to form a seed layer for the under bump metal and to also provide a contact plating (electrical buss) layer. Nikel may be used in lieu of copper for the second layer.

[0028] The next step consists of patterning the wafer with a thick (preferably between 50 - 200 μm) layer of an ultra-violet sensitive photoimagable organic film 16 such as a liquid photoresist or dry film as indicated in Fig. 2(c) which is deposited by spinning it onto the surface of the wafer following by baking to harden the layer, or by lamination of the dry film. To produce such a thickness with liquid resists, a two-step application and baking may be required. The photosensitive layer is then patterned by exposing it through a metal-coated glass photomask which has openings selectively etched in the metal layer to define the areas to be bumped. These openings allow ultra-violet light to pass through and expose the photosensitive layer. The thickness of the photosensitive layer and the size of the opening determines in part the final volume and shape of the solder bump. The thickness is important to ensure sufficient bump height is obtained to ensure sufficient chip stand-off from the substrate after the bump is reflowed and flip-chip bonded. Either positive or negative tone photosensitive polymers may be used for this process. After developing the photosensitive layer, which provides a protective layer to areas that are not to be plated, electrical contacts points are opened at the edges of the wafer to the underlying sputtered copper layer and the wafer is then plated with either copper (or nickel) to form the under-bump-metal (UBM) 18 as indicated in Fig. 2(d). This layer which is normally between 3-7 μm thick acts as a "wettable" foundation to the solder bump.

[0029] The wafer is then electroplated with solder (Fig. 3(a)) and by selecting the appropriate type of plating solution and anodes in the plating bath, lead-free deposits of pure tin, or alloys comprising tin-copper, tin-silver, or tin-bismuth bumps 20 can be formed from a single plating solution with simultaneous co-deposition of the respective elements in the desired stoichiometry. Plating solutions from a variety of providers can be employed, for example those of Shipley Ronal. For pure tin electroplating Shipley Ronal's "Tinglo Culmo" product is particularly appropriate, whilst for tin-bismuth their "Solderon BI" product is appropriate. A negative voltage is usually applied to the wafer effectively making it the cathode. For each of these desired alloys either a pure tin anode or tin-copper anode is utilized in the case of a soluble anode technique, or for tin-bismuth deposition an insoluble platinized titanium anode is preferred. The tin-copper, tin-bismuth, and tin-silver plated deposits can be formed either from a single plating solution with simultaneous co-deposition of the respective elements in the desired stoichiometric amounts or by sequential plating of the pure elements (in the desired amounts) followed by reflow of the plated deposit to achieve an alloy with the desired composition. An applied current density of 3-5 A.S.D (amps per square decimetre) is found to be appropriate. Either direct current (DC) or pulse-plating techniques can be used in conjunction with rack or fountain (cup) plating equipment. For D.C. plating 3-5V with a current of between 0.05 to 0.1A is preferred. For a pulsed alternating current, a pulse comprising about +5V for about 1 millisecond, followed by

zero V for about 1 millisecond, followed by -5V for 1 millisecond, followed by zero V for 1 millisecond is found to be beneficial in terms of bump uniformity and composition of the deposit.

[0030] It has also been found that instead of simultaneously depositing the respective elements from a single plating solution, the pure elements may be deposited by sequentially plating from separate plating solutions, and controlling the plating time to control the relative amounts of each element. Whilst this results in a layered structure of the pure elements, when the plated deposit is reflowed (as discussed further below) the resultant bump is an alloy of the desired stoichiometry. This sequential plating can be employed for any of the binary alloys discussed. It is found to be generally unimportant which element is plated first and which second.

[0031] In the case of tin-silver-copper this sequential technique is found to be particularly useful, as plating of ternary alloys from a single plating solution is difficult owing to the difficulty in accurately controlling the resultant alloy composition. In this case a tin-copper deposit is preferably formed separately from the silver by first simultaneously co-depositing tin-copper from a single binary plating solution, followed by plating of pure silver. On reflow of the as-plated deposits the desired ternary alloy is formed. Alternatively, the silver may be deposited first, followed by plating of tin-copper. As a further alternative, the three individual elements may be sequentially deposited. This option is viable for deposition of relatively large bumps, but becomes more difficult with smaller bumps owing to the fact that the proportion of copper is small (less than 2%, and preferably about 0.7%), and accurate control of the amount of deposited copper becomes then more difficult.

[0032] If the plating process is stopped before the solder reaches the top of the patterned photosensitive layer, the bump will form a pillar shape (Fig. 3(a1). If the plating process is continued above the height of the photoresist, a "mushroom" shape will form (Fig. 3(a)). Mushrooming can be used if necessary to increase the volume of the solder in instances where it is not possible to pattern the photosensitive layer to the desired height.

[0033] Further steps in completing the bump fabrication process involve removal of the protective photosensitive layer as shown in Fig. 3(b) and back-etching of the sputtered copper and chrome layers using chemical means as indicated in Fig. 3(c).

[0034] Flux is then applied to the as-plated bumps and they are re-flowed in an oven to form the spherical solder shape 20'. Alternatively a flux-less reflow of the bump can be achieved when using a combination of a reducing nitrogen and hydrogen environment.

[0035] The particular selected bump solder materials are as follows:

a) Pure Tin

This is selected because it is the simplest, cheapest, and easiest to fabricate as a lead-free replacement for lead-tin bumps, and yet has fairly similar physical, electrical and thermal characteristics to lead-tin solder. It also has a low toxicity and good solderability.

Despite the fact that there is a strong prejudice against using pure tin in microelectronic packages due to the well-documented effect of formation over time of tin whiskers (which can cause shorting and device failure), the use as solder bump for a flip-chip application does not suffer the problem of whisker formation. It is believed that whisker formation is a stress-time dependent effect, and it is believed the reflow process relieves this stress.

b) Tin-Copper

The percentage of copper must be less than 2wt% and preferably in the region of about 0.7wt% which represents the eutectic point, this composition exhibiting a melting point of 227°C. Concentrations of copper much greater than about 2% are undesirable as they have an increased melting point (which increases fabrication problems) and because copper forms intermetallic compounds with tin which are brittle and therefore mechanically unstable. The tin-copper alloy system with a composition of 99.3wt%Sn/0.7wt%Cu with a melting point of 227°C can be considered as a lead-free replacement for high-lead (95wt%Pb/5wt%Sn or 97wt%Pb/3wt%Sn) alloys which have melting points in excess of 300°C. The tin-copper alloy systems could also be considered as a replacement for eutectic lead-tin bumps if the substrate is able to tolerate a reflow temperature of about 260°C.

c) Tin-Silver

The percentage of silver for most applications must be less than 5%wt and preferably 3.5%wt which is the eutectic point of the alloy system. Small additions of silver may be desired since they have shown to significantly increase the ductility of pure tin which may be desirable in cases where the bumps may be subjected to stress and multiple thermal cycling. Concentrations of silver higher than 3.5%wt are typically not desirable due to the high cost of silver. Moreover, the melting point of the Sn-Ag system increases rapidly with increasing silver content. For example, at the eutectic point of 3.5%wt silver the melting point is 221°C. At 10%wt silver the melting point is 300°C which is too high for most low-cost organic substrate or packaging materials. However, in cases where a high melting point (in excess of 300°C) lead-free solder bump is desired, such as for flip-chip bonding onto ceramic substrates, a silver composition of less than 20% and more preferably about 10% is preferred. At 20% silver the melting point is about 375°C which is potentially useful for certain high temperature applications, although at 10% silver the melting point is

about 300°C which is comparable to the melting point of existing 95wt%Pb/5wt%Sn and 95wt%Pb/3wt%Sn alloys. Thus, the eutectic (96.5wt%Sn/3.5wt%Ag) and high-silver (90wt%Sn/10wt%Ag) content alloys can be considered as lead-free replacements of eutectic (37wt%Pb/63wt%Sn) and high-lead (95wt%Pb/5wt%Sn or 97wt%Pb/3wt%Sn) alloys respectively.

d) Tin-Bismuth

The percentage of bismuth is selected to be in the range of 10-25%wt. The tin-bismuth system exhibits an acceptable melting point over a wide range of compositions; 225°C at 10% Bi and 138°C at 60% (which represents the eutectic point). At about 20%wt bismuth, the melting point of the Sn-Bi alloy is 185°C which is similar to that of eutectic lead-tin at 183°C so this particular Sn-Bi alloy can therefore be used as a "drop-in" replacement to the eutectic lead-tin solder.

e) Tin-Silver-Copper

The tin-silver-copper alloy has a composition of less than 5wt% silver, preferably in the region of 3.5wt%Ag, less than 2wt% copper, preferably in the region of 0.7wt%Cu, with the balance being tin. This alloy has a melting point of between 216°C and 217°C which makes it suitable as a substitute for eutectic lead-tin solders.

[0036] The above-described elemental tin and tin alloy compositions applied by electroplating are found to produce solder bumps which are lead free whilst having properties compatible with those of conventional lead-tin solder bumps.

[0037] Figure 4(a) is a scanning electron micrograph of eutectic tin-copper bumps as-plated, whilst Figure 4 (b) shows these after reflow, showing highly regular well-defined bumps.

[0038] Figures 5(a) and (b) are scanning electron micrographs of tin-bismuth solder bumps for 90wt%Sn: 10wt%Bi, also exhibiting regular well-defined solder bumps of appropriate height for bonding to a substrate.

[0039] Figures 6(a) and (b) are scanning electron micrographs of as-plated and after reflow pure tin solder bumps.

[0040] Figures 7(a) and (b) are scanning electron micrographs of the as-plated and after reflow tin-silver solder bumps for 96.5wt%Sn:3.5wt%Ag showing regular well-defined solder bumps.

[0041] Figures 8(a) and (b) are scanning electron micrographs of the as-plated and after reflow tin-silver-copper solder bumps for 95.7wt%Sn:3.5wt%Ag: 0.8%Cu fabricated using the method of sequential plating of tin-silver followed by tin-copper.

Claims

1. A method of forming solder bumps on a chip or wafer for flip-chip applications, comprising the steps of providing a chip or wafer having a plurality of metal bonds pads which provide electrical connection to the chip or wafer, and applying a solder bump comprising pure tin or a tin alloy selected from tin-copper, tin-silver, tin-bismuth, or tin-silver-copper by an electroplating technique, and melting the solder bumps by heating to a temperature above the bump melting point to effect reflow.

2. A method according to claim 1 wherein the solder is tin-copper alloy having less than 2% by weight copper, the balance being tin.

3. A method according to claim 2 wherein the solder is tin-copper alloy having about 0.7% by weight copper.

4. A method according to claim 1 wherein the solder is tin-silver alloy having less than 20% by weight silver, the balance being tin.

5. A method according to claim 4 wherein the tin-silver alloy has about 3.5% by weight silver, the balance being tin.

6. A method according to claim 4 wherein the tin-silver alloy has about 10% by weight silver, the balance being tin.

7. A method according to claim 1 wherein the solder is tin-bismuth having between 5 and 25% by weight bismuth, the balance being tin.

8. A method according to claim 7 having about 20% by weight bismuth, the balance being tin.

9. A method according to claim 1 wherein the solder is tin-silver-copper alloy having less than 5wt% silver and less than 2wt% copper, the balance being tin.

10. A method according to claim 9 having about 3.5wt% silver.

11. A method according to claim 9 having about 0.7wt% copper.

12. A method according to claim 1 wherein the elements of the tin-copper, tin-silver or tin-bismuth alloys are simultaneously co-deposited as the alloy from a single plating solution.

13. A method according to claim 1 wherein the tin-copper, tin-silver, tin-bismuth or tin-silver-copper alloys

are deposited by sequentially plating pure elements, which form the requisite alloys on heating.

14. A method according to claim 1 wherein the tin-silver copper alloy is deposited by depositing one or other of tin-copper alloy from a single plating solution by co-deposition, or elemental silver, followed by deposition of the other, the ternary alloy forming on heating.

15. A method according to claim 1 wherein the chip or wafer is provided with a layer of thick photosensitive material patterned to define the location of the solder bumps, the photosensitive material being of between 25 and 200 μm thickness.

16. A method according to claim 1 wherein the electroplating is carried out using a direct current.

17. A method according to claim 1 wherein the electroplating is carried out using a pulsed alternating current.

18. A method according to claim 17 wherein each pulse comprises about +5V for about 1 millisecond, zero voltage for about 1 millisecond, about -5V for about 1 millisecond, followed by zero voltage for about 1 millisecond.

19. A method for forming solder bumps on a chip or wafer for flip-chip applications comprising the steps of:

(a) providing a chip or wafer having a passivation layer and a plurality of exposed metallic bond pads;
(b) applying at least one solder-wettable metal layer to the bond pad;
(c) applying a photosensitive layer to the chip or wafer having openings at the portions of the bond pads;
(d) applying a solder comprising pure tin, or a tin alloy selected from tin-copper, tin-silver, tin-bismuth or tin-silver-copper by an electroplating technique;
(e) removing the photosensitive layer; and
(f) melting the solder bumps to effect reflow.

20. A chip or wafer having solder bumps formed according to the method of claim 1.

21. A chip or wafer having solder bumps formed according to the method of claim 19.

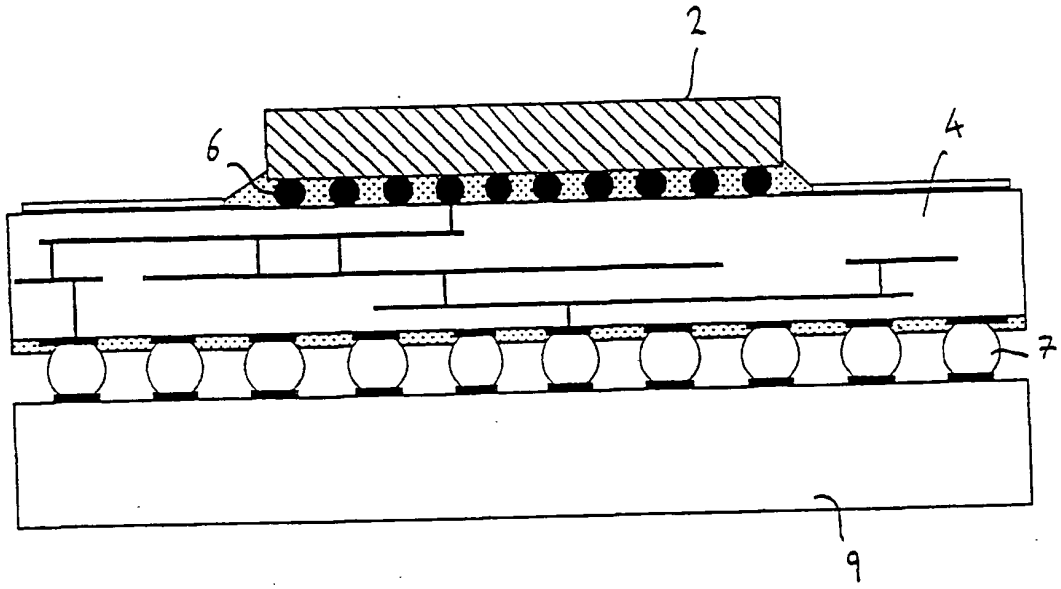
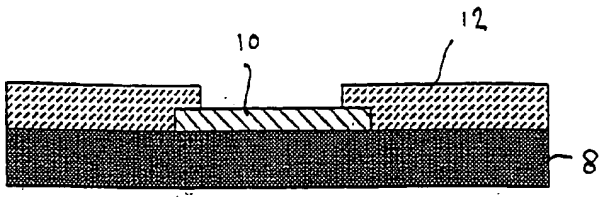
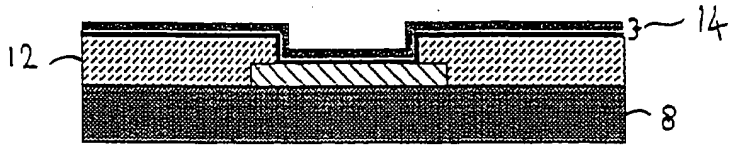


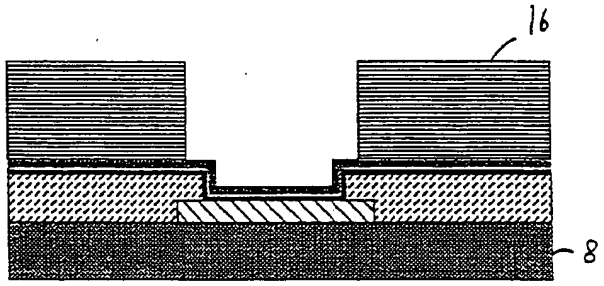
FIG. 1



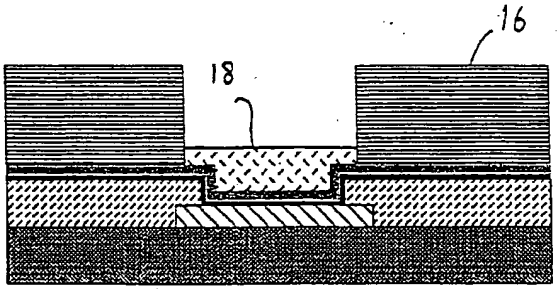
(a)



(b)



(c)



(d)

FIG. 2

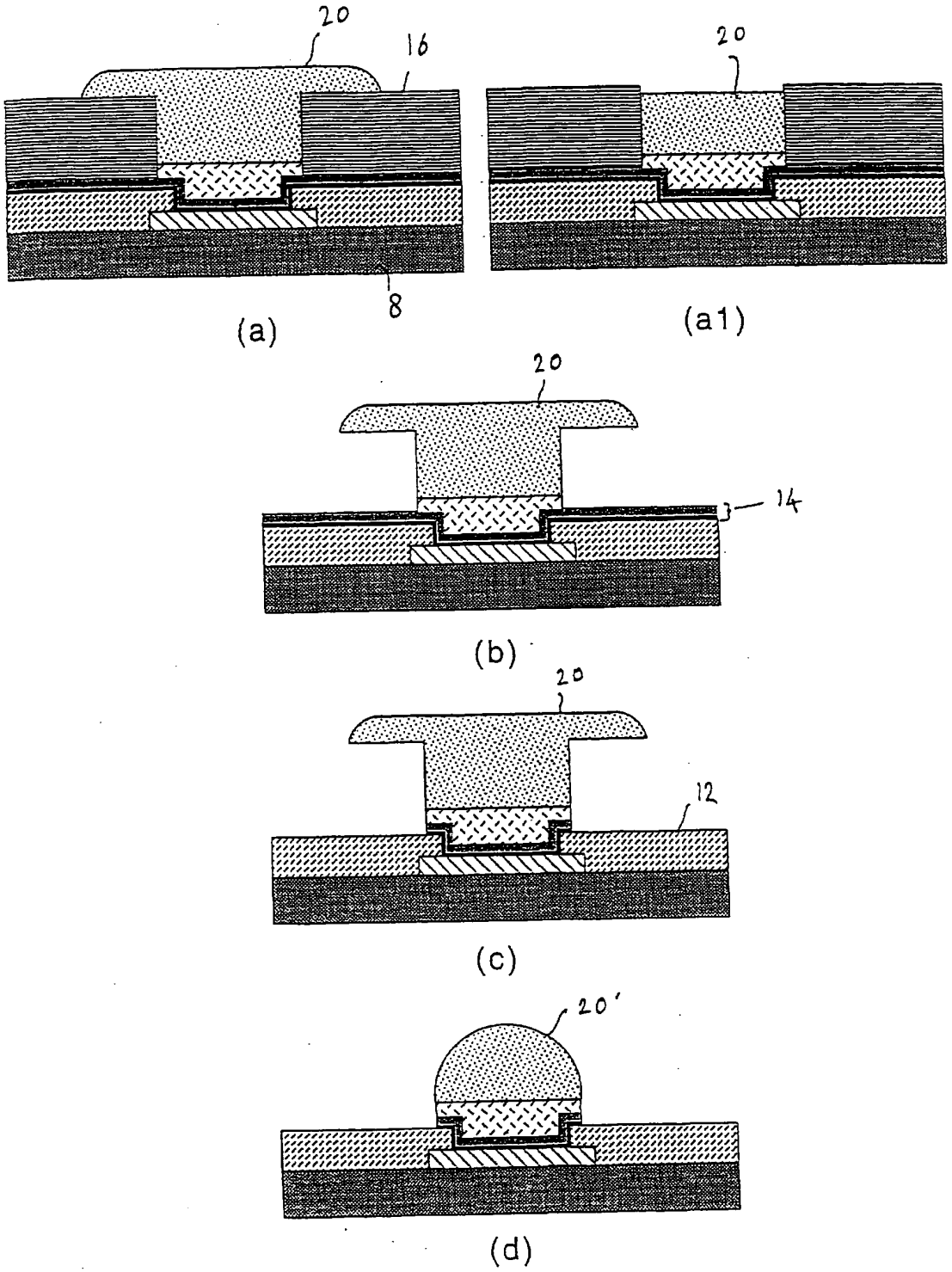


FIG. 3

Lead-Free Sn:Cu (99.3:0.7) Bumps as-plated

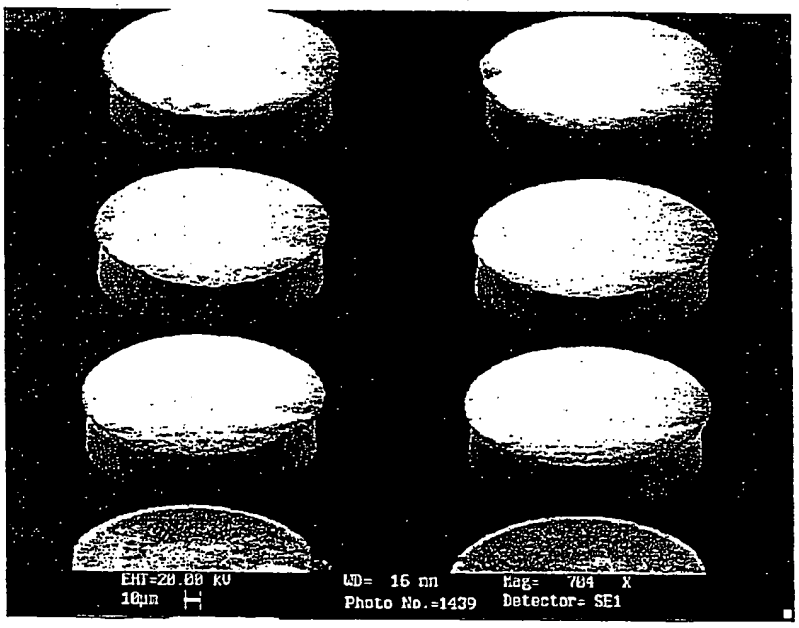


FIG. 4(a)

after reflow

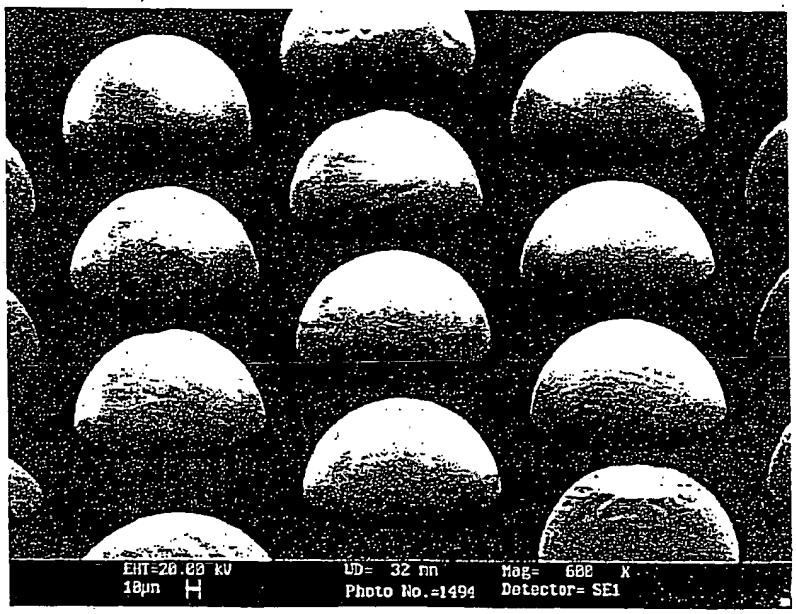


FIG. 4(b)

Lead-Free Sn:Bi (90:10) Bumps

as-plated

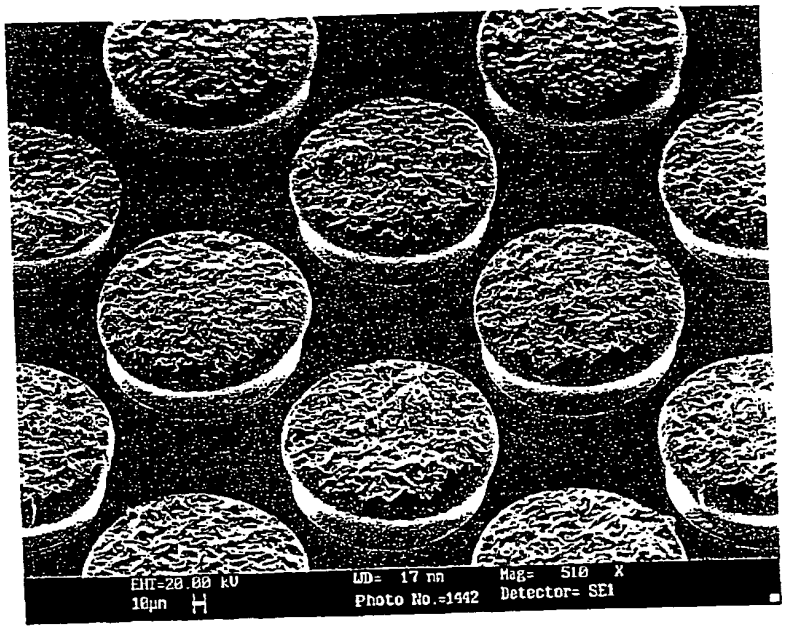


FIG. 5(a)

after reflow

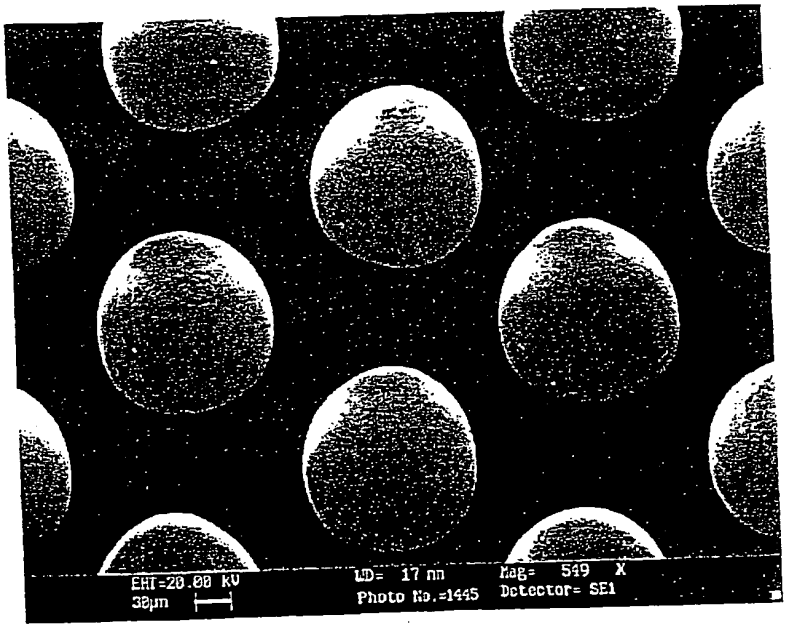


FIG. 5(b)

Lead-Free Pure-Tin Bumps

as-plated

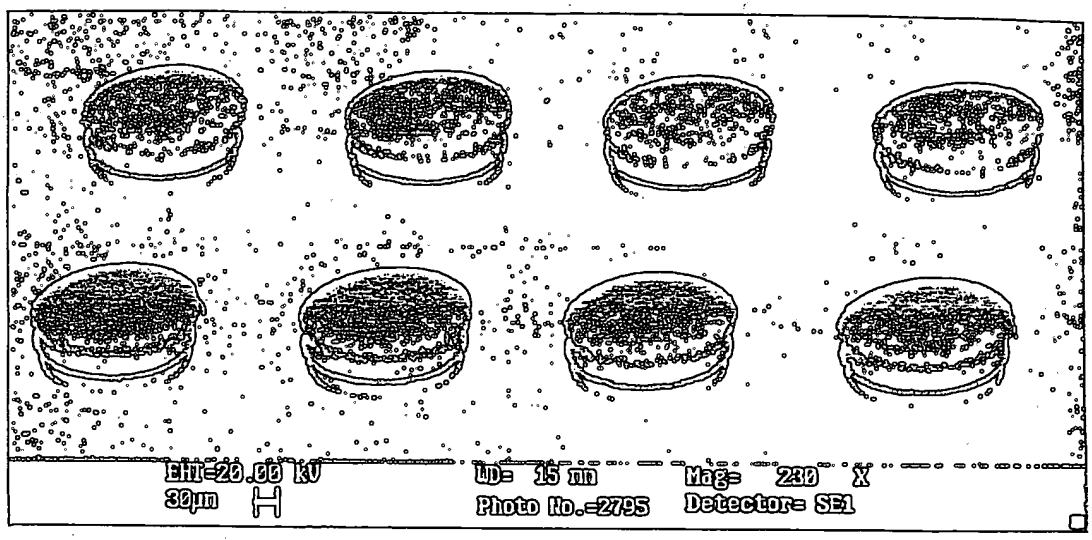


FIG. 6(a)

after reflow

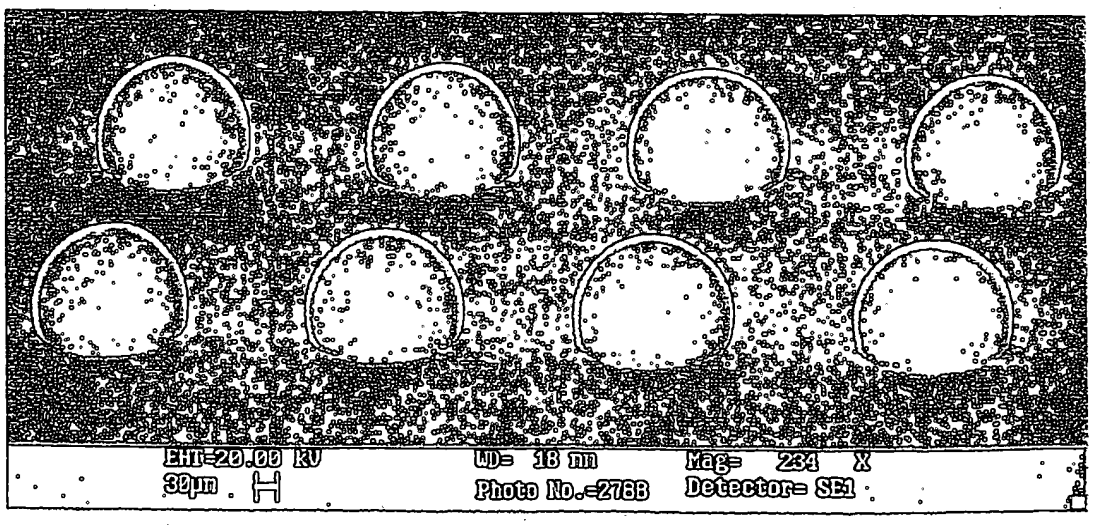


FIG. 6(b)

Lead-Free Sn:Ag (96.5:3.5) Bumps

as-plated

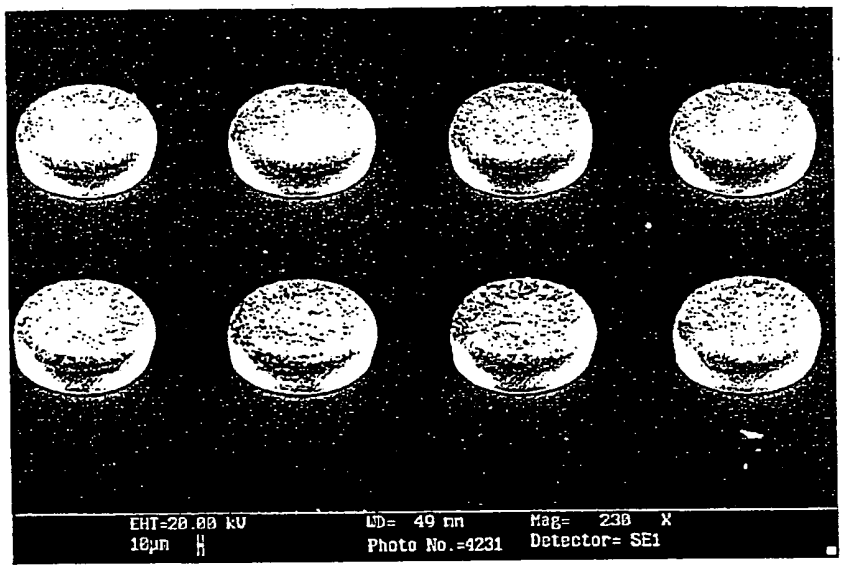


FIG. 7(a)

after reflow

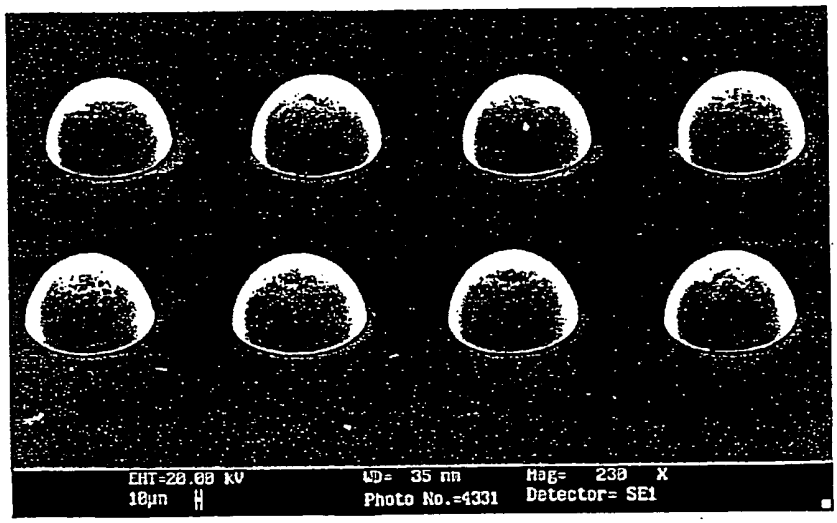


FIG. 7(b)

Lead-Free Sn:Ag:Cu (95.7:3.5:0.8) Bumps

as-plated

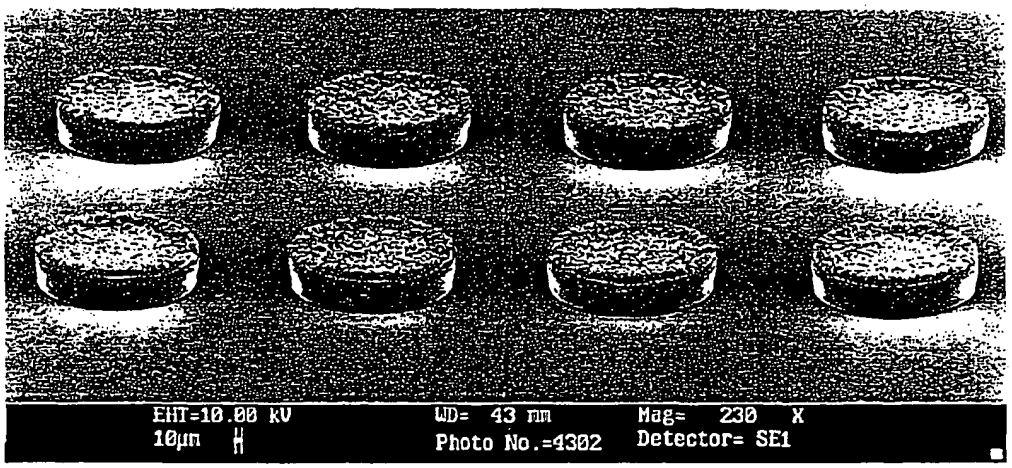


FIG. 8(a)

after reflow

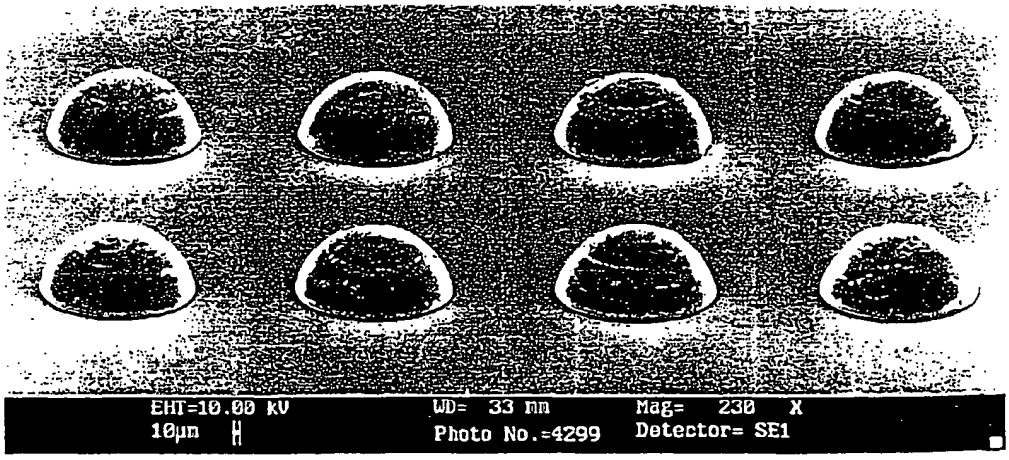


FIG. 8(b)

(19) Europäisches Patentamt
European Patent Office
Office européen des brevets

(11) EP 1 148 548 A3

(12) # EUROPEAN PATENT APPLICATION

(88) Date of publication A3:
30.01.2002 Bulletin 2002/05

(51) Int Cl.7: **H01L 23/485**

(43) Date of publication A2:
24.10.2001 Bulletin 2001/43

(21) Application number: **01302292.6**

(22) Date of filing: **13.03.2001**

(84) Designated Contracting States:
AT BE CH CY DE DK ES FI FR GB GR IE IT LI LU MC NL PT SE TR
Designated Extension States:
AL LT LV MK RO SI

(30) Priority: **19.04.2000 US 552560**

(71) Applicant: **Advanced Interconnect Technology Ltd.**
Tsuen Wan, Hong Kong (HK)

(72) Inventors:
- **Cheung, Edwin Wai Ming**
  Tsuen Wan, Hong Kong (HK)
- **Karim, Zaheed Sadrudin**
  New Territories Hong Kong (HK)

(74) Representative:
Watkin, Timothy Lawrence Harvey
Lloyd Wise, Tregear & Co., Commonwealth House, 1-19 New Oxford Street
London, WC1A 1LW (GB)

(54) **Method of forming lead-free bump interconnections**

(57) A method of forming solder bumps on a chip or wafer for flip-chip applications comprises the steps of providing a chip or wafer having a plurality of metal bonds pads which provide electrical connection to the chip or wafer, and applying a solder bump comprising pure tin or a tin alloy selected from tin-copper, tin-silver, tin-bismuth or tin-silver-copper by an electroplating technique, and melting the solder bumps by heating to a temperature above the bump melting point to effect reflow.

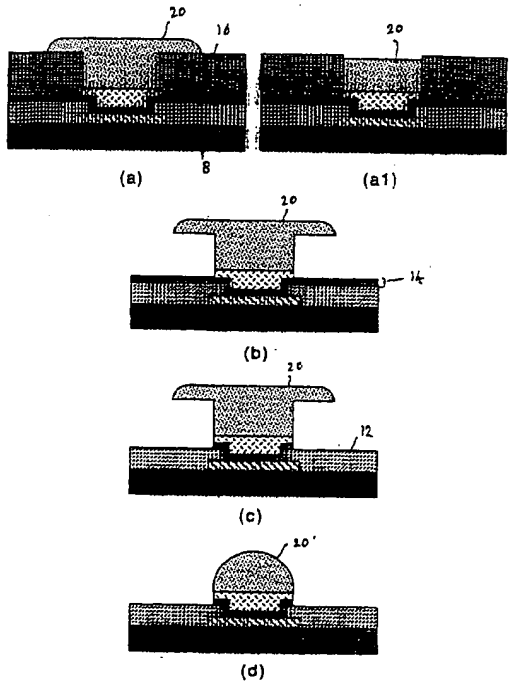


FIG. 3

EP 1 148 548 A3

European Patent Office

EUROPEAN SEARCH REPORT

Application Number
EP 01 30 2292

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.7)
X Y	US 6 013 572 A (PARK JONG-HAN ET AL) 11 January 2000 (2000-01-11) * column 3, line 60 - column 7, line 48; figure 5 *	1,13,15, 19-21 2-11	H01L23/485
X Y	EP 0 818 563 A (NAGANO PREFECTURE ;SHINKO ELEC IND (JP)) 14 January 1998 (1998-01-14) * page 13; example 27 *	1,4-6, 12,16, 17,20,21 2-11	
Y	DE 198 27 014 A (KURODA DENKI KABUSHIKI GAISHA ;TOSHIBA KAWASAKI KK (JP)) 24 December 1998 (1998-12-24) * example 8 *	2,3	
Y	DE 198 16 671 A (FUJI ELECTRIC CO LTD) 22 October 1998 (1998-10-22) * page 10, line 30 - page 12, line 26; table 3 *	4-6,9-11	
Y	PATENT ABSTRACTS OF JAPAN vol. 2000, no. 06, 22 September 2000 (2000-09-22) -& JP 2000 068410 A (NISHIHARA RIKO KK), 3 March 2000 (2000-03-03) * abstract *	7,8	TECHNICAL FIELDS SEARCHED (Int.Cl.7) H01L B23K C25D
Y	US 5 039 576 A (WILSON HAROLD P) 13 August 1991 (1991-08-13) * column 2, line 10-26 * * column 9, line 25-35; figure 1 *	7,8	
A	PATENT ABSTRACTS OF JAPAN vol. 2000, no. 05, 14 September 2000 (2000-09-14) -& JP 2000 054189 A (FURUKAWA ELECTRIC CO LTD:THE), 22 February 2000 (2000-02-22) * abstract *	1	

-/--

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
MUNICH	6 December 2001	Edmeades, M

CATEGORY OF CITED DOCUMENTS

X : particularly relevant if taken alone
Y : particularly relevant if combined with another document of the same category
A : technological background
O : non-written disclosure
P : intermediate document

T : theory or principle underlying the invention
E : earlier patent document, but published on, or after the filing date
D : document cited in the application
L : document cited for other reasons

& : member of the same patent family, corresponding document

EPO FORM 1503 03.82 (P04C01)

European Patent Office

EUROPEAN SEARCH REPORT

Application Number
EP 01 30 2292

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.7)
A	EP 0 825 281 A (LUCENT TECHNOLOGIES INC) 25 February 1998 (1998-02-25) * the whole document *	18	
A	US 5 851 482 A (KIM CHANG-JOO) 22 December 1998 (1998-12-22) * tables 1-1,2-1 *	7,8	

TECHNICAL FIELDS SEARCHED (Int.Cl.7)

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
MUNICH	6 December 2001	Edmeades, M

CATEGORY OF CITED DOCUMENTS

X : particularly relevant if taken alone
Y : particularly relevant if combined with another document of the same category
A : technological background
O : non-written disclosure
P : intermediate document

T : theory or principle underlying the invention
E : earlier patent document, but published on, or after the filing date
D : document cited in the application
L : document cited for other reasons

& : member of the same patent family, corresponding document

EPO FORM 1503 03.82 (P04C01)

ANNEX TO THE EUROPEAN SEARCH REPORT ON EUROPEAN PATENT APPLICATION NO. EP 01 30 2292

This annex lists the patent family members relating to the patent documents cited in the above-mentioned European search report. The members are as contained in the European Patent Office EDP file on
The European Patent Office is in no way liable for these particulars which are merely given for the purpose of information.

06-12-2001

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 6013572 A	11-01-2000	KR 219806 B1	01-09-1999
		JP 3004959 B2	31-01-2000
		JP 10335364 A	18-12-1998
EP 0818563 A	14-01-1998	AU 1556297 A	22-08-1997
		EP 0818563 A1	14-01-1998
		KR 268967 B1	16-10-2000
		US 5902472 A	11-05-1999
		EP 0893514 A2	27-01-1999
		JP 3034213 B2	17-04-2000
		JP 9296274 A	18-11-1997
		WO 9728296 A1	07-08-1997
DE 19827014 A	24-12-1998	JP 11010385 A	19-01-1999
		DE 19827014 A1	24-12-1998
		US 6123248 A	26-09-2000
DE 19816671 A	22-10-1998	JP 10286689 A	27-10-1998
		JP 11058066 A	02-03-1999
		DE 19816671 A1	22-10-1998
		US 6179935 B1	30-01-2001
		JP 11077366 A	23-03-1999
JP 2000068410 A	03-03-2000	NONE	
US 5039576 A	13-08-1991	NONE	
JP 2000054189 A	22-02-2000	NONE	
EP 0825281 A	25-02-1998	US 5750017 A	12-05-1998
		EP 0825281 A1	25-02-1998
		JP 3222409 B2	29-10-2001
		JP 10096095 A	14-04-1998
		SG 53044 A1	28-09-1998
US 5851482 A	22-12-1998	KR 182412 B1	01-04-1999
		KR 182410 B1	01-04-1999
		KR 182411 B1	01-04-1999

EPO FORM P0459

For more details about this annex : see Official Journal of the European Patent Office, No. 12/82

This Page is Inserted by IFW Indexing and Scanning Operations and is not part of the Official Record

BEST AVAILABLE IMAGES

Defective images within this document are accurate representations of the original documents submitted by the applicant.

Defects in the images include but are not limited to the items checked:

- ☐ BLACK BORDERS
- ☐ IMAGE CUT OFF AT TOP, BOTTOM OR SIDES
- ☐ FADED TEXT OR DRAWING
- ☑ BLURRED OR ILLEGIBLE TEXT OR DRAWING
- ☐ SKEWED/SLANTED IMAGES
- ☐ COLOR OR BLACK AND WHITE PHOTOGRAPHS
- ☐ GRAY SCALE DOCUMENTS
- ☐ LINES OR MARKS ON ORIGINAL DOCUMENT
- ☐ REFERENCE(S) OR EXHIBIT(S) SUBMITTED ARE POOR QUALITY
- ☐ OTHER: _____

IMAGES ARE BEST AVAILABLE COPY.

As rescanning these documents will not correct the image problems checked, please do not report these problems to the IFW Image Problem Mailbox.